Midterm Exam

(Due date: February 15th)

Presentation and clarity are very important! Show your procedure!

Problem 1 (20 pts)

- Compute the result of the following operations. The operands are signed fixed-point numbers. The result must be a signed fixed point number. For the division, use $x = 5$ fractional bits.

1.0001 + 1.001001	1000.0101 - 1.010101	01.11111 + 0.00001
01.011 × 1.01101	1.001 × 1.0101	01.01110 ÷ 1.011

Problem 2 (12 pts)

- Represent these numbers in Fixed Point Arithmetic (signed numbers). Select the minimum number of bits in each case.
  - ✓ -16.3125
  - ✓ 37.375

- Complete the table for the following fixed point formats (signed numbers): (6 pts.)

Integer bits	Fractional Bits	FX Format	Range	Resolution
6	2			
8	4			

Problem 3 (36 pts)

- Calculate the result (provide the 32-bit result) of the following operations with 32-bit floating point numbers. Truncate the results when required. When doing fixed-point division, use 4 fractional bits. Show your procedure.

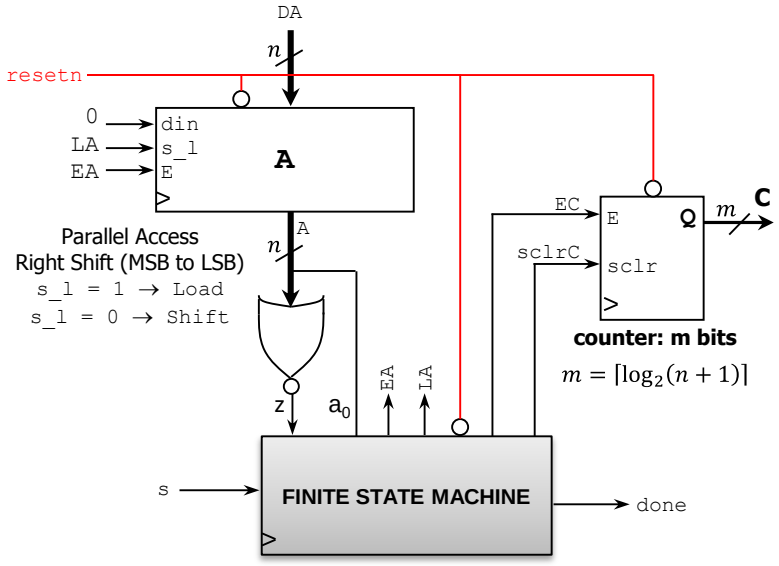
✓ 42FA8000 + C0E00000	✓ 50DAD000 – D0FAD000	✓ 01800000 × FAB80000	✓ 7B390000 ÷ C8C00000

Problem 4 (32 pts)

- "Counting 1's" Circuit: It counts the number of bits in register A that has the value of '1'.
  The digital system is depicted below: FSM + Datapath. Example: For $n = 8$: if $A = 00110110$, then $C = 0100$.
  - ✓ m-bit counter: $sclr$. If $E = sclr = 1$, the count is initialized to zero. If $E = 1, sclr = 0$, the count is increased by 1.
  - ✓ Parallel access shift register: If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift.

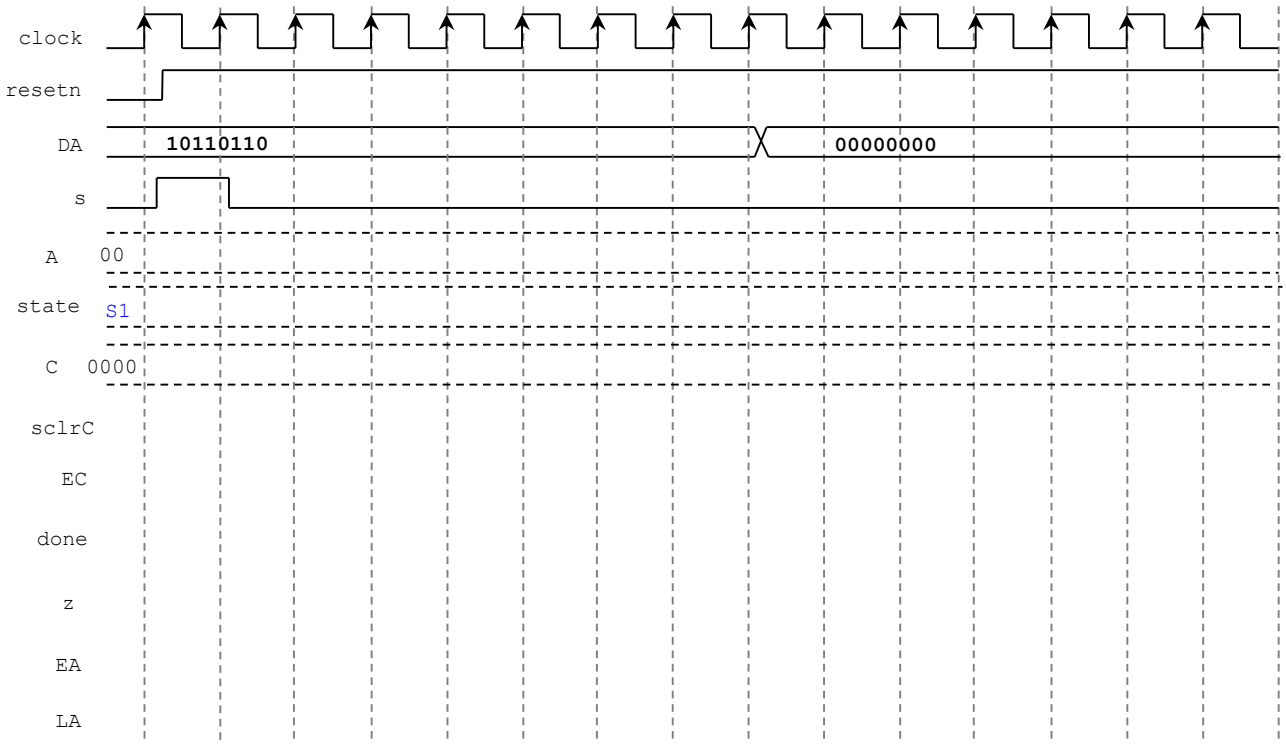
- Sketch the Finite State Machine diagram (in ASM form) given the algorithm. (20 pts.)
  - ✓ The process begins when s is asserted, at this moment we capture DA on register A. Then the process starts by shifting A one bit at a time. The process is concluded when $A = 0$. The signal $done$ is asserted when we finish counting.
  - ✓ Note: If $A = 0 \rightarrow z = 1$, if $A \neq 0 \rightarrow z = 0$. As A is being shifted, every time $a_0 = 1$, we need to increase the count C.

- Complete the timing diagram (next page) where $n = 8, m = 4$. (12 pts.)



ALGORITHM

```
C ← 0
while A ≠ 0
   if a0 = 1 then
      C ← C + 1
   end if
   right shift A
end while
```


clock
resetn
DA
10110110
00000000
s
A
00
state
S1
C
0000
sclrC
EC
done
z
EA
LA